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EXAMINER	
LINDSAY JR, WALTER LEE	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,362	JUENGLING ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-45 and 64-91* is/are pending in the application.

4a) Of the above claim(s) *34-45,64-69 and 87-91* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-31,33,70-76,80,81 and 84-86* is/are rejected.

7)☒ Claim(s) *32,77-79,82 and 83* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Election filed on 9/21/2004.

Currently claims 22-45 and 64-91 are pending. Claims 34-45, 64-69 and 87-91 are withdrawn from consideration.

Election/Restrictions

1. Applicant's election without traverse of claims 22-33 and 70-86 in the reply filed on 9/21/2004 is acknowledged.

2. Claims 34-45, 64-69 and 87-91 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected method, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 9/21/2004.

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 24, 26, 29-30 and 85-86 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claims 24 and 29 recite the limitation "said conducting layer" in line 2. There is insufficient antecedent basis for this limitation in the claims.

For examination purposes "said conducting layer" is viewed as the "polysilicon layer" of independent claim 22.

7. Claim 85 recites the limitation "said polysilicon layer" in lines 13-14. There is insufficient antecedent basis for this limitation in the claim.

For examination purposes "said polysilicon layer" is viewed as the "said conducting layer" from line 5 of claim 85.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 22-24, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Song (U.S. Patent No. 5,686,331, dated 11/11/1997).

Song shows the structure as claimed in Figs. 2A-2I and corresponding text as: a semiconductor substrate (1) (Fig. 2A)(col. 2, lines 46-47); a gate stack provided over

said substrate, said gate stack comprising: a gate oxide layer (10) provided on said substrate (Fig. 2A) (col. 2, lines 46-47)[gate insulating layer is gate oxide, due to the fact that one of the objectives is to maintain the quality of the gate oxide (col. 1, lines 66-col. 2, line 20)]; a polysilicon layer (11) provided on said gate oxide layer (Fig. 2B) (col. 2, lines 48-49)[gate electrode is polysilicon due to the fact layer 19 is formed by reacting a metal to the gate electrode to form a polysilicide layer (col. 3, lines 16-20)]; at least one unetched silicide layer (19) formed over and in contact with said polysilicon layer (Fig. 2I) (col. 3, lines 13-24) [silicide layer is unetched only the unreacted metal is removed]; and source and drain regions (4) provided in said substrate on opposite sides of said gate stack (Fig. 2D) (col. 2, lines 52-58) (claim 22). Song teaches that the structure comprises first sidewall spacers (13) on sidewalls of said gate stack (Fig. 2E)(col. 2, lines 59-62) (claim 23). Song teaches that the structure comprises second sidewall spacers (14) provided over and at edges of said conducting layer (Fig. 2I) (col. 3, lines 13-24) (claim 24). Song teaches that the silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof (col. 3, lines 25-34) (claim 33).

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 22-23 and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu (U.S. Patent No. 6,287,925, filed 2/24/2000).

Yu shows the structure as claimed in Fig. 1 and corresponding text as: a semiconductor substrate (102)(col. 1, lines 34-45); a gate stack provided over said substrate, said gate stack comprising: a gate oxide layer (116) provided on said substrate (col. 1, line 66-col. 2, line 4); a polysilicon layer (118) provided on said gate oxide layer (col. 1 lines 46-55); at least one unetched silicide layer (120) formed over and in contact with said polysilicon layer (col. 1, lines 46-55); and source (110) and drain (112) regions provided in said substrate on opposite sides of said gate stack (col. 1, lines 46-55) (claim 22). Yu teaches that the structure comprises first sidewall spacers (124) on sidewalls of said gate stack (col. 1, line 66-col. 2, line 4)(claim 23). Yu teaches that the silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof (col. 7, lines 34-44) (claim 33).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. Claims 25-26, 29, 70-71, 74 and 75-76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song (U.S. Patent No. 5,686,331, dated 11/11/1997) in view of Yu et al. (U. S. Patent No. 6,180,468, dated 1/30/2001).

Song shows the structure substantially as claimed and as described in the preceding paragraphs. Additionally, Song shows that the structure further comprises second sidewall spacers provided over and at edges of said conducting layer (Fig. 2I) (col. 3, lines 13-24) (claim 29). Additionally, Song shows the structure as claimed in Figs. 2A-2I and corresponding text as: a semiconductor substrate (1) (Fig. 2A)(col. 2, lines 46-47); a gate stack provided over said substrate, said gate stack comprising: a gate oxide layer (10) provided on said substrate (Fig. 2A) (col. 2, lines 46-47); a conducting layer (11) provided on said gate oxide layer; (Fig. 2B) (col. 2, lines 48-49); first sidewall spacers (13) provided on sidewalls of said gate stack (Fig. 2E)(col. 2, lines 59-62); at least one unetched silicide layer (19) formed over and in contact with said polysilicon layer (Fig. 2I) (col. 3, lines 13-24); and source and drain regions (4) provided in said substrate on opposite sides of said gate stack (Fig. 2D) (col. 2, lines 52-58) (claims 70 and 75). Song teaches that the conducting layer is polysilicon (col. 3, lines 13-24) (claims 71 and 76). Song teaches that the silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof (col. 3, lines 25-34) (claim 74).

Song lacks anticipation only in not explicitly teaching that: 1) the structure comprises at least one channel implant region in said substrate below said gate stack,

which is defined at least in part by said first sidewall spacers (claim 25); and 2) the structure comprises at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers (claim 26); 3) the structure comprises at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said first sidewall spacers (claim 70); and 4) the structure comprises at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers (claim 75).

Yu et al. teaches the formation of a MOS transistor with a very low thermal budget implant process. Yu et al. teaches a channel implant (38) that is self-aligned to a polysilicon gate by using nitride spacers (32 and 34) to control implantation (col. 3, lines 29-41). Yu et al. teaches that the channel implant is implanted through a gate oxide layer into the underlying silicon substrate. (col. 3, lines 29-41). The channel implant provides for a very sharp doping profile and good immunity to short-channel effects such as threshold voltage roll-off, drain-induced-barrier-lowering and source/ drain punch-through. The implant is also spaced away from the source/drain to avoid increasing parasitic junction capacitance.

It would be obvious to one of ordinary skill in the art, at the time the invention was made, to modify the structure shown in Song by implementing at least one channel implant region that is in part defined by the first sidewall spacers or in part defined by the second sidewall spacers, as taught in Yu et al., with the motivation that Yu et al. teaches that the channel implant defined by the sidewall spacers provide for a very

sharp doping profile and good immunity to short-channel effects, such as threshold voltage roll-off, drain-induced-barrier-lowering and source/drain punch-through. Additionally, Yu et al. teaches that the channel implant is spaced away from the source/drain to avoid increasing parasitic junction capacitance.

14. Claims 25, 70-71 and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (U.S. Patent No. 6,287,925 filed 2/24/2000) in view of Yu et al. (U.S. Patent No. 6,180,468 dated 1/30/2001).

Yu shows the structure as claimed and as described in the preceding paragraphs. Additionally, Yu shows the structure as substantially claimed in Figs. 1 and corresponding text as: a semiconductor substrate (102) (col. 1, lines 34-45); a gate stack provided over said substrate, said gate stack comprising: a gate oxide layer (116) provided on said substrate (col. 1, line 66 -col. 2, line 4); a conducting layer (118) provided on said gate oxide layer; (col. 1, lines 46-55); first sidewall spacers (122) provided on sidewalls of said gate stack (col. 1 line 66-col. 2, line 4); at least one unetched silicide layer (120) formed over and in contact with said polysilicon layer (col. 2, lines 46-55); and source (110) and drain regions (112) provided in said substrate on opposite sides of said gate stack (col. 1, line 46-55) (claims 70). Yu teaches that the conducting layer is polysilicon (col. 1, lines 46-55) (claim 71). Yu teaches that the silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof (col. 7, lines 33-44) (claim 74).

Yu lacks the anticipation of not explicitly teaching that: 1) the structure further comprises at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said first sidewall spacers (claim 25); 2) the structure comprises at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said first sidewall spacers (claim 70)

Yu et al. teaches the formation of a MOS transistor with a very low thermal budget implant process. Yu et al. teaches a channel implant (38) that is self-aligned to a polysilicon gate (col. 3, lines 29-41). The channel implant provides for a very sharp doping profile and good immunity to short-channel effects such as threshold voltage roll-off, drain-induced-barrier-lowering and source/ drain punch-through. The implant is also spaced away from the source/drain to avoid increasing parasitic junction capacitance.

It would be obvious to one of ordinary skill in the art, at the time the invention was made, to modify the structure shown in Yu by implementing at least one channel implant region that is in part defined by the first sidewall spacer, as taught in Yu et al., with the motivation that Yu et al. teaches that the channel implant defined by the sidewall spacers provides for a very sharp doping profile and good immunity to short-channel effects, such as threshold voltage roll-off, drain-induced-barrier-lowering and source/drain punch-through. Additionally, Yu et al. teaches that the channel implant is spaced away from the source/drain to avoid increasing parasitic junction capacitance.

15. Claims 27, 28, 31, 72-73, 80-81 and 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (U.S. Patent No. 6,287,925 filed 2/24/2000) in view of Yu et al. (U.S. Patent No. 6,180,468 dated 1/30/2001) as applied to claims 23, 25 70 and portions of 80, and further in view of Tseng et al. (U.S. Patent No. 6,043,545 dated 3/28/2000).

Yu as modified by Yu et al. show the structure as substantially claimed in the preceding paragraphs. Additionally, Yu shows the structure as substantially claimed in Figs. 1 and corresponding text as: a semiconductor substrate (102) (col. 1, lines 34-45); a gate stack provided over said substrate, said gate stack comprising: a gate oxide layer (116) provided on said substrate (col. 1, line 66 -col. 2, line 4); a conducting layer (118) provided on said gate oxide layer; (col. 1, lines 46-55); first sidewall spacers (122) provided on sidewalls of said gate stack (col. 1 line 66-col. 2, line 4); at least one unetched silicide layer (120) formed over and in contact with said polysilicon layer (col. 2, lines 46-55); and source (110) and drain regions (112) provided in said substrate on opposite sides of said gate stack (col. 1, line 46-55) (claim 80). Yu teaches that the conducting layer is polysilicon (col. 1, lines 46-55) (claim 81). Yu teaches that the silicide layer is formed of a material in the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof (col. 7, lines 33-44) (claim 84).

Yu as modified by Yu et al. lack the anticipation of not explicitly teaching that: 1) the structure comprises an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack (claim 27 and 72); 2)

the structure comprises at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said area (claims 28 and 73); 3) the structure comprises an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack (claim 31); and 4) the structure comprises an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack; and at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said area (claim 80).

Tseng teaches a MOSFET device with First sidewall spacers (206) or (210) and insulating layer (214). Tseng teaches the etching away of the first liner oxide spacer (206) (Fig 2F to Fig. 2G) to expose the top and sides of the gate(204) (col. 3, line 64-col. 4, line 3), and also teaches the etching away of the top portion of the insulating layer 214 (Fig. 2E to Fig. 2F). Tseng does this to reduce gate-induced dual leakage and to protect the transistor from short channel effects (col. 2, lines 6-19).

It would be obvious to one of ordinary skill in the art, at the time the invention was made, to modify the structure, shown in the combination of Yu, as modified by Yu et al., by implementing an insulating layer adjacent to the first sidewall spacers, the insulating layer and the first sidewall spacers having etched out upper portions, as taught by Tseng, with the motivation that Tseng teaches that by etching the upper portion of the

spacers and insulating layer, the gate induced dual leakage is reduced and the transistor is protected from short channel effects.

Allowable Subject Matter

16. Claims 32, 77-79, and 82-83 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. Claims 30 and 86 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

18. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said area, as required by claim 32, as it depends from claim 31;

...further comprising an insulating layer adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack, as required by claim 77, as it depends from claim 75;

...further comprising at least one channel implant region in said substrate below said gate stack, which is defined at least in part by said area, as required by claim 78, as it depends from claim 77;

...wherein said silicide layer is formed of a material in the group consisting of W, WSix, WN, Ti, TiN, and other combinations thereof, as required by claim 79, as it depends from claim 77.

...further comprising second sidewall spacers provided over and at edges of said conducting layer, as required by claim 82, as it depends from claim 80; and

...further comprising at least another channel implant region in said substrate below said gate stack, which is defined at least in part by said second sidewall spacers, as required by claim 83, as it depends from claim 82.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
October 27, 2004